

Enterprise Project Management for the Semiconductor Industry

a PLM Whitepaper
Prepared by ENOVIA MatrixOne, Inc.

Executive Summary

Semiconductor companies that can continuously deliver a steady stream of winning designs to market stand to gain substantial long-term competitive advantage. But while many companies are able to create breakthrough products, they struggle to do so in a consistent, continuous, and timely manner.

Very often semiconductor companies are forced to make tradeoffs between chip development projects, sacrificing speed and quality in one project to accommodate success in another. With rapidly changing customer requirements and ever-shrinking product shelf lives, winning semiconductor companies will be those that can easily manage multiple complex chip development projects across a distributed design chain of internal employees, IP vendors, and design partners.

ENOVIA MatrixOne, Inc. has responded to this need for extended enterprise project management across the IC design chain with an enterprise project management solution tailored to the ways in which IC design chains function. The ENOVIA MatrixOne solution takes into account the workflows and processes of chip design teams as well as the challenges that they face on a day-to-day basis.

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Business Challenges

As today's IC design and production teams attempt to simultaneously manage and control a wide variety of chip development projects and programs, they are confronted with the following challenges:

- Management has few, if any, early warning signs of troubled chip design projects to help remove barriers and keep them on track.
- There is a lack of accountability and traceability between design phase handoffs. This often results in downstream phase owners receiving the blame for delays resulting from incomplete upstream phase deliverables.
- It is often difficult to know if the right person or right skill set is being applied at the right time across project teams.
- Project members are working with outdated or low-quality information.
- Projects teams are not using standardized processes across business units and/or sites.
- Determining overall project status is a tedious manual process.

The prevalence of these conditions can impede chip development projects and negatively impact business in numerous ways:

- Chip development is delayed, because resources are not properly allocated
- Design project decisions are based on outdated information
- Market opportunities are missed as a result of delays
- Costly re-spin occurs as incorrect data sets are sent to the mask shop
- Delivery penalties are imposed, cutting into profit margins
- Customer dissatisfaction and/or customer loss increase
- Project results are unpredictable or late

While it is unlikely that a chip producer incurs all of these problems simultaneously, without good project management tools in place, the risk of these problems and their business consequences are increased. Use of good project management tools and methodologies significantly mitigates such risks.

The ENOVIA MatrixOne Solution

ENOVIA MatrixOne has a proven track record of addressing the business challenges outlined above. Through our multi-pronged solution for Enterprise Project Management (EPM), chip makers can improve productivity of both the design process, as well as the entire product development process, from concept to silicon. The EPM solution leverages several key MatrixOne technologies:

- MatrixOne Program Central™
- MatrixOne Semiconductor Accelerator™
- Synchronicity Developer Suite™ (featuring DesignSync® and ProjectSync®)

Program Central enables companies to efficiently manage complex programs and projects that rely on extensive collaboration across global value chains of employees, customers, suppliers and partners. Through project dashboards, this application provides management with real-time visibility into a project's status in terms of process, costs and benefits and allows decision makers to

easily determine which projects have the highest probability for success.

The Semiconductor Accelerator provides a sample stage gate model implementing a hierarchical group of standard IC design flow templates, as well as an overarching program view of the entire concept-to-silicon process. The design flow templates include the following elements:

- IC-Digital Flow
- Digital IC Front End Flow (specification, RTL, verification)
- Layout Flow (place & route, prototype, system test, extraction, DRC)
- IC-Analog/Custom Flow (schematics, layout, DRC, extraction, verification)
- IC-Astro Place and Route Flow
- IC-CMOS Manufacturing Process
- IC-Microprocessor Flow
- IC-ASIC Flow
- IC-Memory Flow
- IC-FPGA Design Flow

While every company has its own unique methods and phases for accomplishing projects, the design flow templates serve as useful starting points from which users easily configure Program Central.

The program view supports numerous templates for new product introduction (NPI), including the following:

- NPI-Phase0 Concept Development
- NPI-Phase1 Business Analysis
- NPI-Phase2 Initial Development
- NPI-Phase3 Final Development
- NPI-Phase4 Product Systems Update
- NPI-Phase5 Product Follow Up

These templates cover the product lifecycle surrounding the chip design stage with incorporation

of such tasks as Feasibility Assessment, Procurement Activities, Cost Analysis and Plan Development.

The Semiconductor Accelerator also provides a set of check lists for defining IP blocks in accordance with VSIA recommendations for soft IP.

Finally, the **Synchronicity Developer Suite**, which features DesignSync and ProjectSync, is ENOVIA MatrixOne's full-featured tool suite for design management, issue tracking and reuse, providing tight integrations to Cadence tools via DesignSync DFlI and Synopsys tools via DesignSync Milkyway. When users of these tools change specific design files, or update their status by way of tagging or flagging ProjectSync notes completed, Program Central will indicate the forward progress on a management dashboard.

ENOVIA MatrixOne Enterprise Project Management at Work

Following is an example of how ENOVIA MatrixOne customers leverage the Enterprise Project Management Solution for Semiconductors to overcome the challenges associated with chip project management. The example focuses on the chip design phases, but the project management features transcend to the program view as well:

Bob, a high level manager at "Big Chip Semiconductor" enters Program Central to gain an overview of all the chips currently under development in his area of responsibility. He views multiple projects, and based upon their color-coded status indicator, he sees that half are "on plan," indicated by a green label and the other half are either "late" (having red labels) or "at risk" (having yellow labels).

Manage Folder/Structure and Project Information Manage and Track Project Schedules Manage and Track Project Costs

Define Team Membership and Communication of Status to Management

Manage and Track Project Issues and Risks

The “at risk” projects labeled in yellow are those that contain unfinished tasks with short-term due dates. Among these, a new custom chip under development has just turned yellow. Bob wants to investigate the causes of the delay, so he expands the new chip’s screen to see its current stage of progress. As he views the progress, he can see that the schematics for the design are not yet ready for layout.

Bob contacts Mary, the schematic designer, who informs him that she is about to complete a Spice simulation and will be ready for layout momentarily. Mary does this by entering into the Cadence DFII environment and referencing the Synchronicity menu to bring up the tag dialog box. She selects “Ready4Layout” and submits the dialog. Soon after, Bob returns to Program Central to find that the Centurion project status indicator has returned to green, or “on plan.”

Continuing through his management dashboard, Bob notices that a second chip under development is now late. He drills further into the screen’s details and finds that the RTL team considers the RTL for the second chip ready for verification but that the verification engineers have not accepted that the second chip is ready for the verification phase. The user interface shows the verification task as red, or “late.” Bob expands this to see an icon representing a “deliverable”, which is a set of files managed in DesignSync. The files need to be in the “Ready4Sim” state but are only in the “Submitted4Sim” state. The UI is accurately reflecting the fact that the RTL designers’ code has not yet achieved formal approval from the verification team. Just at this time, Stuart, the Verification Manager has been reviewing a set of Verilog regression runs to determine if the last submitted RTL code is ready. Stuart goes into Program Central to view the full lifecycle that the RTL code needs to traverse. He advances the state

from “Verification Submitted4Sim” to “Ready4Sim” - signifying his approval. This act causes DesignSync to tag the file set “Ready4Sim”, which is used by downstream processes. Bob sees the task turn green and is ready to proceed once again. Note: If Stuart had not been satisfied, he may just have easily moved the state back to “NotReady”, in which case Program Central would have flagged the task for the RTL team to fix the problems and re-submit (by retagging), delaying the “Ready4Sim” tag.

Next, Bob looks into the progress of various teams by examining planned vs. actual handoff dates. Then Bob runs a resource utilization report by person and sees that Lynn, a verification engineer, is expected to be overcommitted for the coming month. From there he views the projects to which Lynn is assigned and those tasks that form the basis for the overrun. He sees that she is expected to do verification of the second chip project as planned, but due to the late completion of the RTL code on another project, Lynn is now double assigned. He then goes to find the RTL Verification skill in Program Central and sees that there are two other engineers eligible to offload Lynn, so he arranges for the re-assigned project coverage.

Ted is starting a new Digital IC project. He goes into Program Central and starts up a new project. Within Program Central he enters the DesignSync vault URL for the project, creating a link between his data management environment and his project management environment. He then browses for the set of templates to find the one with the appropriate predefined work breakdown structure (e.g IC-digital flow, IC-analog/custom flow, etc.). He selects the IC-Digital Flow. Having chosen the IC-Digital Flow, his new project is now populated with a set of tasks and deliverables that represent the required steps in his project and their outputs. Ted descends into the Specification task and from there views the deliverable for the specification document, which is managed in DesignSync.

Addressing the Business Challenges

We will conclude by relating this sample scenario back to the previously outlined business challenges.

Challenge: Management has no early warning signs of troubled chip design projects to help remove barriers and keep them on track.

Solution: Solving this starts with management decomposing the chip design process into its phases, stages and down to specific tasks. Program Central provides a place to capture these tasks with expected completion dates. The Semiconductor Accelerator provides templates for standard design projects to serve as a starting point. A manager who frequents Program Central's dashboards can see at a quick glance which projects are on track, which are not, and where the bottlenecks exist – all in real time.

Challenge: There exists a lack of accountability and traceability between design phase handoffs. A tendency develops to blame downstream phase owners for delays resulting from incomplete upstream deliverables.

Solution: When dealing with the handoff from one design phase to another, it is important to have a signoff process defined. It is not enough for an RTL team to feel that their design is ready for "place and route," the layout group needs to acknowledge that they have provided the proper inputs. Program Central governs the approval of completing a design phase. Moreover, the dates between submittal and approval are all captured, and with this increased visibility raised, correct behavior is encouraged.

Challenge: It is often difficult to know if the right person or right skill set is being applied at the right time across project teams.

Solution: Program Central provides a place to record the various skills that each person may contribute to a project. For each skill, management can see which employees possess the skill, how long employees have practiced the skill, and employees' competency levels. When planning projects, project managers can run reports which show the current resource utilization across projects. This, combined with the ability to view the skill sets of available personnel, enables optimal resourcing of projects. As numerous projects continue toward completion, the resource picture can change. Resource utilization reports show yellow/red indicators highlighting overcommitted months coming, permitting optimal balancing of personnel.

Challenge: Project members are working with outdated or poor quality information, and determining overall project status is a tedious manual process.

Solution: Without a web based tool to track process steps, a manager's only recourse to get the needed information is to ask each individual about his/her own task status. With Program Central, everyone has access to the system, and people would generally prefer not to have a visible hub reflect old information. Furthermore, DesignSync users who need to check-in or tag data for downstream user reference need no extra steps to update status. Thus, a Cadence user, for example, can spend all day in Virtuoso®, and management is automatically kept up-to-date on the project's status.

Challenge: Projects teams are not using standardized processes across business units / sites.

Solution: Use of Program Central encourages standardization. The system makes it much easier for upper management to edict standard flows. The key is for upper management to define the critical points of visibility that are needed for all the projects they oversee. Within these, project teams have the freedom to manage more granular tasks, so long as they roll up to the standard phases and milestones. In time, a library of best practices can be factored out as repeatable templates for other projects to follow.

Conclusion

ENOVIA MatrixOne Enterprise Project Management for the Semiconductor Industry provides management with visibility into IC design projects by connecting design data management with program management across the entire semiconductor design chain. This ensures that multiple complex IC design projects stay on schedule and maintain optimal product quality.

Semiconductor companies leveraging ENOVIA MatrixOne's solution drive consistency, continuity, and speed into their processes while remaining focused on what they do best – creating breakthrough new designs for an increasingly demanding market.

About ENOVIA MatrixOne

MatrixOne, Inc. was acquired by Paris-based Dassault Systemes in May, 2006 and today is part of its ENOVIA PLM Collaborative Environment family of solutions. The ENOVIA MatrixOne solutions enable companies to accelerate product innovation to achieve top line revenue growth and improve bottom line profitability. ENOVIA MatrixOne is focused on helping companies across the automotive, aerospace & defense, consumer, machinery, medical device, semiconductor and high-tech industries solve their most challenging new product development and introduction problems. More than 850 companies use ENOVIA MatrixOne solutions to drive business value and gain a competitive advantage, including industry leaders such as BAE Systems, Bosch, Comau, General Electric, Honda, Johnson Controls, Linde AG, NCR, New Balance, Nokia, Philips, Porsche, Procter & Gamble, REI, Sony Ericsson, STMicroelectronics and Toshiba. ENOVIA MatrixOne (www.matrixone.com) is headquartered in Westford, Massachusetts, with locations throughout North America, Europe and Asia-Pacific.



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