

Advanced Micro Devices

Improving reliability of flip-chips with Abaqus FEA from SIMULIA



Overview

■ Challenge

Advanced Micro Devices (AMD) needed a way to predict and prevent crack formation and delamination in the flip-chip version of its integrated circuits

■ Solution

AMD chose Abaqus FEA from SIMULIA to study the effects various underfill design variables

■ Benefits

Thanks to complex studies conducted with Abaqus FEA, AMD came up with a list of improvements to the underfill layer, which optimized flip-chip reliability and durability



"We chose Abaqus because of its powerful fracture mechanics capabilities."

Zhen Zhang
Senior Packaging Engineer
AMD

AMD

Flip-chips: chip-of-choice

Only 50 years after its invention, it is hard to imagine life without the integrated circuit (IC). As the heart - or the brain - of all computers, ICs power the world's most complex systems in communications, manufacturing, and transportation. A significant and growing part of this market is the flip-chip.

Developed in the 1960s by IBM and used initially in mainframes, flip-chips are mounted face-down, or flipped, directly onto a substrate, circuit board, or carrier. As compared with their wire-bonded cousins, flip-chips are small and can reduce circuit board area by up to 95 percent, improve processing speed, are less expensive in high-volumes, and are more reliable because they are more rugged.

Because of these advantages, flip-chips have become the chip-of-choice for many portable, cost-conscious applications such as watches, smart cards, cellular telephones, pagers, and a variety of portable consumer electronics. But like any enabling technology, flip-chips still have their design and manufacturing

challenges, and improvements in reliability are still possible.

It is no surprise, therefore, that finite element analysis (FEA) is being used by leading technology innovators such as Advance Micro Devices (AMD) in the ongoing development and improvement of chip design. AMD is a global supplier of integrated circuits for personal and networked computing and communications, based in Sunnyvale, California.

Preventing underfill failure is critical

"In flip-chip packages, the mismatch in coefficients of thermal expansion of the various layers induces stresses that can result in delamination," said Zhen Zhang, Senior Packaging Engineer, AMD. Especially critical is the underfill, a layer of adhesive between the chip and substrate that locks together the two layers. Once locked, the electrical contact is maintained, the contact bumps are protected from moisture and other environmental hazards, and the assembly has added mechanical strength. "However,



imperfect underfill with voids or microcracks will produce delamination under temperature cycling conditions,” Zhang noted.

To help predict and prevent such delamination, the engineering team at AMD used Abaqus FEA from SIMULIA. The team studied the effect of various underfill design variables that could potentially play a role in crack formation and delamination. “We chose Abaqus because of its powerful fracture mechanics capabilities,” said Zhang. “In addition, it has other features - such as contact mechanics, global-local submodeling routines, surface-to-surface tie constraints, a variety of partition and meshing tools, and parametric GUI and Python scripting for high productivity - all of which were useful in this study.”

FEA models help examine underfill behavior

To study delamination, engineers at AMD used the FEA software to create a parametric model of the flip-chip capable of automatic crack generation. For its analysis, the group focused on temperature excursion or cycling, the cause of many failures. “We used Abaqus/CAE to build the models,” said Zhang, who took full advantage of the software’s flexibility and automation features. “We modified the journal files into Python scripts and defined the parameters - including geometries, material properties, and loading conditions - for fully

parameterized studies. We also used scripting/automation in CAE to post-process the simulation results and output them into Excel files.”

Simulation provides 3D fracture results and design recommendations

For the purposes of the study, Zhang’s group inserted a crack at the corner of the interface between the chip and the underfill layer and then examined the effect of a number of variables on crack generation. “This complex analysis was possible thanks to the parametric capabilities of the Abaqus model,” Zhang noted. “Analyzing the effect that certain variables have on crack generation enabled us to come up with a list of improvements to the underfill layer that would optimize reliability and durability.”

Making future flip-chips even better

Zhang, who has been studying flip-chips for two years, has already made significant recommendations and design improvements using FEA. “The analysis provided reliable data for all flip-chips in which underfill is incorporated - from package to board level, and from assembly to service conditions,” he said. Looking to the future, Zhang noted that such analysis guides both materials selection and design and assembly optimization, and concluded, “The impact on future flip-chip design is positive.”

“This complex analysis was possible thanks to the parametric capabilities of the Abaqus model, and the impact on future flip-chip design is positive.”

Zhen Zhang
Senior Packaging Engineer
AMD



Dassault Systèmes
10, rue Marcel Dassault
78140 Vélizy Villacoublay – France
+33 (0)1 61 62 61 62



SolidWorks®, CATIA®, DELMIA®, ENOVIA®, SIMULIA® and 3DVIA® are registered trademarks of Dassault Systèmes or its subsidiaries in the US and/or other countries.

Images courtesy of AMD

© Copyright Dassault Systèmes 2010
All Rights Reserved

For more information or to contact a sales representative, please visit www.3ds.com/contact